This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (Currently Amended) A data switch for communicating among a plurality of devices coupled to said data switch in a digital data network wherein a virtual connection is represented by a connection between a first device of said plurality of devices and a second device of said plurality of devices of said digital data network, said switch including:

a switch element having a switch matrix, the switch element including a plurality of buffer structures, said plurality of buffer structures being configured to allow buffering to be accomplished on a per-virtual connection basis;

at least one input switch access port structure coupled to said switch element ~~matrix~~ containing a plurality of input back pressure buffer structures, wherein said plurality of input back pressure buffer structures is configured to allow input back pressuring to be accomplished on a per-virtual connection basis;

a plurality of input ports coupled to said at least one input switch access port structure, wherein said plurality of input ports are coupled to a plurality of traffic generators; and

at least one output arbitration structure coupled to said switch matrix and coupled to ~~said~~ a plurality of output ports, wherein said at least one output arbitration device represents ~~the~~ circuitry for arbitrating access to a single output port of said plurality of output ports~~; and~~

~~a plurality of output ports coupled to said output arbitration portion, wherein said plurality of output ports are coupled to a plurality of output destinations~~.

2-6 (Canceled)

7. (Previously presented) The switch of claim 1 wherein a size of said plurality of input back pressure buffer structures are individually set.

8. (Previously presented) The switch of claim 1, wherein a size of a single input back pressure buffer structure of said plurality of input back pressure buffer structures is optimized by specifying a threshold window which includes a maximum and minimum size for said input back pressure buffer structure.

9. (Currently Amended) The switch of claim 1, wherein a size of said plurality of input back pressure buffer structures is configured for a plurality of ~~said~~ virtual connections.

10. (Previously Presented) The switch of claim 9, wherein said plurality of input back pressure buffer structures are configured for said plurality of virtual connections having a same priority.

11. (Previously presented) The switch of claim 1, wherein each output arbitration structure of said at least one output arbitration structure includes a plurality of schedulers and a plurality of selectors.

12. (Previously presented) The switch of claim 11, wherein each scheduler of said plurality of schedulers is configured to schedule ATM cells on one of a per-virtual connection basis, a per-port basis, a per traffic class, a per priority basis, a per group of virtual connections basis, and a cells similarly grouped basis.

13. (Previously presented) The switch of claim 11, wherein arbitration is performed on a per-virtual connection basis wherein said each scheduler of said plurality of schedulers are coupled to connections having a same priority for switching.

14. (Previously presented) The switch of claim 11, wherein each scheduler of said plurality of schedulers is coupled to at least two buffer structures having a same priority.

15. (Previously presented) The switch of claim 11 wherein each selector of said plurality of selectors is configured to select ATM cells using at least one of a round-robin selection technique and a weighted round-robin technique.

16. (Previously presented) The switch of 11, wherein said at least one output arbitration structure includes one of said plurality of selectors for every ATM output.

17. (Currently Amended) A data switch for communicating among a plurality of devices coupled to said data switch in a digital data network wherein a virtual connection is represented by a connection between a first device of said plurality of devices and a second device of said plurality of devices of said digital data network, said switch including:

a switch element having a switch matrix, the switch element including a plurality of buffer structures, said plurality of buffer structures being configured to allow buffering to be accomplished on a per-virtual connection basis;

at least one input switch access port structure coupled to said switch element ~~matrix~~ containing a plurality of input back pressure buffer structures, wherein said plurality of input back pressure buffer structures is configured to allow input back pressuring to be accomplished on a per-virtual connection basis;

a plurality of input ports coupled to said at least one input switch access port structure, wherein said plurality of input ports are coupled to a plurality of traffic generators; ~~and~~

at least one output switch access port structure coupled to said switch element ~~matrix~~ containing a plurality of output buffer structures, said plurality of output buffer structures being configured to allow output buffering to be accomplished on a per-virtual connection basis~~, said at least one output switch access structure including,~~

~~a plurality of schedulers,~~

~~a at least one selector,~~

~~an at least one switch matrix output port~~; and

at least one output port coupled to said at least one output switch access port structure, wherein said at least one output port is coupled to a plurality of output destinations~~;~~

~~wherein said at least one output switch access structure arbitrates access to a respective said at least one output port~~.

18. (Previously presented) The switch of claim 17 wherein a size of said plurality of input back pressure buffer structures are individually set.

19. (Previously presented) The switch of claim 18 wherein a size of a single input back pressure buffer structure of said plurality of input back pressure buffer structures is optimized by specifying a threshold window which includes a maximum and minimum size for said input back pressure buffer structure.

20. (Currently Amended) A data switch for communicating among a plurality of devices coupled to said data switch in a digital data network wherein a virtual connection is represented by a connection between a first device of said plurality of devices and a second device of said plurality of devices of said digital data network, said switch including:

a switch element having a switch matrix, the switch element including a plurality of buffer structures, said plurality of buffer structures being configured to allow buffering to be accomplished on a per-virtual connection basis;

at least one input switch access port structure coupled to said switch ~~matrix~~ element containing a plurality of input back pressure buffer structures, wherein said plurality of input back pressure buffer structures is configured to allow input back pressuring to be accomplished on a per-virtual connection basis, and a size of a single input back pressure buffer structure of said plurality of input back pressure buffer structures is optimized by specifying a threshold window which includes a maximum and minimum size for said input back pressure buffer structure, and a size of said plurality of input back pressure buffer structures are individually set;

~~a plurality of~~ at least one output switch access port structure ~~structures~~ coupled to said switch element ~~matrix~~ containing a plurality of output buffer structures, said plurality of output buffer structures being configured to allow output buffering to be accomplished on a per-virtual connection basis;

~~a plurality of input ports coupled to said plurality of switch access port structures, wherein said plurality of input ports are coupled to a plurality of traffic generators;~~

~~a plurality of output ports coupled to said switch matrix, wherein said plurality of output ports are coupled to a plurality of output destinations;~~ and

at least one output arbitration device defined in the switch element and coupled to said switch matrix ~~and coupled to said plurality of output ports~~, wherein said at least one output arbitration device represents ~~the~~ circuitry for arbitrating access to a single output port of a ~~said~~ plurality of output ports of the switch element.

21. (Previously presented) The switch of claim 20, wherein said at least one output arbitration device schedules cells inputted into said input ports in accordance to a weight accorded to each cell of said plurality of cells.

22. (Previously presented) A switch element, comprising:

an input routing portion including a switch matrix input port for receiving data;

a buffer portion including a plurality of buffers;

a switch matrix portion for routing data out from the plurality of buffers;

an output arbitrating portion, including,

a plurality of schedulers for receiving the data from the plurality of buffers through the switch matrix,

a selector for receiving data from the plurality of schedulers, the selector enabling output from the switch element through a switch matrix output port.

23. (Currently Amended) ~~A~~ The switch element as recited in claim 22, further comprising:

an additional input routing portion including an additional switch matrix input port for receiving data;

an additional buffer portion including an additional plurality of buffers, the switch matrix portion routing data out from the additional plurality of buffers;

an additional output arbitrating portion, including an additional plurality of schedulers for receiving the data from the additional plurality of buffers through the additional switch matrix, and

an additional selector for receiving data from the additional plurality of schedulers, the additional selector enabling output from the switch element through an additional switch matrix output port.

24. (Currently Amended) ~~A~~ The switch element as recited in claim 23, wherein the output arbitrating portion receives data from the buffer portion and the additional buffer portion through the switch matrix portion and the additional switch matrix portion.

25. (Currently Amended) ~~A~~ The switch element as recited in claim 24, wherein the additional output arbitrating portion receives data from the buffer portion and the

additional buffer portion through the switch matrix portion and the additional switch matrix portion.

26. (Currently Amended) ~~A~~ The switch element as recited in claim 22, wherein the input routing portion receives data from a plurality of traffic generators.

27. (Currently Amended) ~~A~~ The switch element as recited in claim 23, wherein a plurality of traffic acceptors receive data from an ~~the~~ output arbitrating structure.

28. (Previously presented) A switch element, comprising:

a first input routing portion including a first switch matrix input port for receiving data;

a first buffer portion including a first plurality of buffers;

a switch matrix portion for routing data out from the first plurality of buffers and a second plurality of buffers;

a first output arbitrating portion, including,

a first plurality of schedulers for receiving the data from the first plurality of buffers and the second plurality of buffers through the switch matrix,

a first selector for receiving data from the first plurality of schedulers, the first selector enabling output from the switch element through a first switch matrix output port;

a second input routing portion including a second switch matrix input port for receiving data;

a second buffer portion including the second plurality of buffers;

a second output arbitrating portion, including,

a second plurality of schedulers for receiving the data from the first plurality of buffers and the second plurality of buffers through the switch matrix,

a second selector for receiving data from the second plurality of schedulers, the second selector enabling output from the switch element through a second switch matrix output port;

a plurality of traffic generators for inputting data into the first input routing portion and the second input routing portion; and

a plurality of traffic acceptors to receive data from the first output arbitrating portion and the second output arbitrating portion.